I CLAIM:

1. A post-processing method for use in a sampled data read channel of a mass data storage device that has a Viterbi detector that receives actual sampled partial response target data from a said data medium of a mass data storage device and produces a recovered data output signal, comprising:

filtering an a recovered partial response target signal derived from said recovered data output signal and said sampled partial response target data to produce a filtered output signal;

providing a threshold circuit to provide a threshold against which said filtered output signal is compared;

generating an error event pattern indicating signal when a predetermined error event pattern occurs in said recovered data output signal;

and modifying the recovered data output signal when said filtered output signal exceeds the threshold of said threshold circuit and said error event indicating signal is generated.

2. The method of claim 1 wherein said Viterbi detector is an EPR4 Viterbi detector.

3. The method of claim 1 wherein said Viterbi detector is an EEPR4 Viterbi detector.

4. The method of claim 1 wherein said error event pattern is ex = ±{1}.

5. The method of claim 1 wherein said error event pattern is ex = ±{1-11}.

6. The method of claim 1 wherein said error event pattern is ex = ±{1-1}.

7. The method of claim 1 wherein said filtering is accomplished by applying said output to an FIR filter.

8. The method of claim 1 further comprising whitening the recovered data output signal, prior to said filtering, with a whitening filter.

9. A sampled data detection technique for use in a mass data storage device, comprising:

equalizing and sampling a read back signal from a transducer head of said mass data storage device to a partial response level of at least EPR4 to produce an actual sampled partial response target signal;

detecting said actual sampled partial response target signal in a Viterbi detector having a partial response detection level of at least EPR4 to produce a recovered data output signal;

delaying said actual sampled partial response target signal for a time substantially equal to a time required by said Viterbi detector to generate said recovered data output signal from said actual sampled partial response target signal to produce a delayed actual sampled partial response target signal;

converting said recovered data output signal to a partial response level of said actual sampled data output signal to produce a converted recovered partial response target signal;

subtracting said converted recovered partial response target signal from said delayed actual sampled partial response target signal to produce an error signal;

determining the occurrence of a predetermined error event pattern in said recovered data output signal to produce an error event pattern indicating signal;

producing, from said error signal, a detection signal having a magnitude based upon the occurrence of an error event;

comparing said detection signal to a predetermined threshold level, and generating an error correction control signal if said data detection signal is larger than said predetermined threshold level, and said error event pattern indicating signal indicates an occurrence of an error pattern; and

correcting said recovered data output signal to correspond to said predetermined data pattern if said error correction control signal has been generated.

10. The method of claim 9 wherein said equalizing comprises equalizing said read back signal to a partial response level of EPR4, and said detecting comprises detecting said actual sampled partial response target signal in a Viterbi detector having a partial response detection level of EPR4.

11. The method of claim 9 wherein said equalizing comprises equalizing said read back signal to a partial response level of EEPR4, and said detecting comprises detecting said actual sampled partial response target signal in a Viterbi detector having a partial response detection level of EEPR4.

12. The method of claim 9 wherein said producing a detection signal comprises filtering said error signal with an FIR filter.

13. The method of claim 9 further comprising whitening said error signal prior to said producing said detection signal.

14. The method of claim 9 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining the occurrence of ex = ±{1} in said recovered data output signal.

15. The method of claim 9 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining the occurrence of ex = ±{1-11} in said recovered data output signal.

16. The method of claim 9 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining the occurrence of ex = ±{1-1} in said recovered data output signal.

17. The method of claim 9 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining a data sequence having a high likelihood of occurrence.

18. A post-processor circuit for use in a sampled data read channel of a mass data storage device, comprising:

a Viterbi detector that receives an actual sampled partial response target signal from a storage medium of said mass data storage device to produce a recovered data output signal;

an error pattern detector to generate an error pattern event indicating signal if a predetermined error event pattern occurs in said sampled partial response target signal;

a circuit for generating an error signal based upon a difference between said recovered data output signal and a delayed said actual sampled partial response target signal;

a threshold circuit to generate an error correction control signal if a magnitude of said error signal exceeds a predetermined threshold;

and an error correction circuit to modify the recovered data output signal when said error correction control signal and said error event pattern indicating occurrence signal are generated.

19. The circuit of claim 18 further comprising a whitening filter connected to receive said error signal to produce an input signal to said threshold circuit.

20. The circuit of claim 19 wherein said whitening filter has a transfer function, NW(D), that is equal to

$(1+a1*D+a2*D^2+...+an*D^n)/(1+b1*D+b2*D^2+...+bm*D^m)$,

in which a1, a2, . . . an, and b1, b2, . . . bm are coefficients related to a density in which data is recorded in said mass data storage device.

21. The circuit of claim 19 wherein said whitening filter has a transfer function, NW(D), that is equal to

$(1+a1*D+a2*D^2+a3*D^3)/(1+D)$,

in which a1, a2, and a3 are coefficients related to a density in which data is recorded in said mass data storage device.

22. The circuit of claim 18 wherein said predetermined error pattern event is ex = ±{1}.

23. The circuit of claim 18 wherein said predetermined error pattern event is ex = ±{1-11}.

24. The circuit of claim 18 wherein said predetermined error pattern event is ex = ±{1-1}.

25. The circuit of claim 18 wherein said circuit for generating an error signal is an FIR filter

26. The circuit of claim 18 wherein said circuit for generating an error signal is an error pattern matched filter.

27. The circuit of claim 18 wherein said circuit for generating an error signal comprises a whitening noise generator and an FIR filter connected to receive an output of said whitening noise generator.

28. The circuit of claim 18 wherein said Viterbi detector has a partial response level of at least EPR4.

29. The circuit of claim 18 wherein said Viterbi detector has a partial response level of at least EEPR4.